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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/265,819	03/10/1999	MAHITO SHINOHARA	35.C13388	4959

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
WU, DOROTHY	
ART UNIT	PAPER NUMBER
2697	10

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/265,819	SHINOHARA, MAHITO	
	Examiner	Art Unit	
	Dorothy Wu	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 17-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 17-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on June 23, 2003. These drawings are acceptable and have been entered.

Response to Amendment

2. Acknowledgement is made of the amendments to the specification, filed on June 23, 2003. All objections to the specification are hereby withdrawn.

3. Upon cancellation of claims 1-16, the 35 USC 112, second paragraph rejections pertaining to claims 5, 6, 7, 8, 10, 11, 12, 14, and 16 are hereby withdrawn.

Response to Arguments

4. Applicant's arguments filed June 23, 2003 have been fully considered but they are not persuasive.

The applicant has argued: "A notable feature of Claim 17 is the switch that effects switching so that the drive pulse generation circuit generates the drive pulse on the basis of one of the first reference clock signal and the second reference clock signal....Further, none of the other cited references, Yasuda, Hynecek et al., and Roberts et al. are understood to disclose the switch recited in Claim 17." The examiner respectfully disagrees. Yasuda teaches a first synchronizing signal generator (SSG1 **18**) for low resolution operable at a video rate, a second synchronizing signal generator (SSG2 **19**) for high resolution, and a switch (SW **20**) for

switching between the synchronizing signals (col. 4, lines 3-7). Yasuda also teaches that the timing generator **21**, which reads on the drive pulse generation circuit, generates pulses to operate the image pickup sensor **3** on the basis of the synchronizing signals multiplexed by the switch **20**. The admitted prior art teaches a clock signal to determine the timing of the drive pulse of the image sensor (page 1, lines 8-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuda, U.S. Patent 6,130,710, in view of the admitted prior art.

Regarding claim 17, Yasuda teaches a sensor chip comprising an image pickup portion (image pickup sensor **3**) including a plurality of pixels, which reads on the photoelectric conversion elements (col. 4, lines 19-23); a scan circuit (timing generator TG **21**) which reads out a signal from said image pickup portion (image pickup sensor **3**) (col. 4, lines 7-9); a first signal generation circuit (SSG1 **18**) which generates a first control signal, a second control signal coming from a second signal generation circuit (SSG2 **19**), and a switch (SW **20**) which effects switching so that the image signals are read out from the image pickup sensor on the basis of one of the first control signal and the second control signal (col. 4, lines 3-9, and Fig. 1). Yasuda does not teach a sensor chip formed on a single semiconductor chip, a drive pulse generation

circuit which generates a drive pulse for driving said scan circuit, reference clock signals, or a terminal which inputs a clock signal from outside said sensor chip. The admitted prior art does teach a sensor chip formed on a single semiconductor chip and a drive pulse generation circuit that generates a drive pulse for driving said scan circuit (Fig. 1). The admitted prior art also teaches the provision of a reference clock signal, via reference clock wiring **6**, to control the driving of the image sensor (page 1, lines 11-15). As the admitted prior art teaches the inputting of a clock signal from outside said sensor chip (page 1, lines 10-15; Fig. 1), the terminal for inputting the clock signal is also taught. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by Yasuda with the apparatus of the admitted prior art to make a sensor on a semiconductor chip comprising two sources for reference clock signals for driving the image sensor, one on-chip and one off-chip, with a switch for multiplexing which clock signal will drive the sensor. One of ordinary skill would have been motivated to make such a modification to provide the possibility of driving the sensor in high or low resolution modes.

Regarding claim 18, Yasuda teaches first and second pulses coming from first and second control circuits (SSG1 **18** and SSG2 **19**) for reading out the signal from said image pickup portion in first and second modes (col. 4, lines 3-9). The admitted prior art teaches a drive pulse generation circuit for driving said scan circuit and a control signal from outside said semiconductor chip for controlling said drive pulse generation circuit (Fig. 1). The terminal that inputs the control signal is inherently taught.

Regarding claim 19, Yasuda teaches that the first mode is a mode for reading out the signal from said image pickup portion at a resolution lower than that of the second mode (col. 4, lines 3-6).

Regarding claim 20, Yasuda teaches a switch (SW **20**) which effects switching so that the image sensor is driven on the basis of one of the signals generated by the first signal synchronizing generator (SSG1 **18**) and the signals generated by the second signal synchronizing generator (SSG2 **19**) (col. 4, lines 3-9). Yasuda does not teach a drive pulse generation circuit formed on a single semiconductor chip comprising a drive pulse generation circuit which generates a drive pulse; the use of reference clock signals; or a terminal which inputs a second reference clock signal from the external of said drive pulse generation chip. The admitted prior art does teach a drive pulse generation circuit formed on a single semiconductor chip comprising a drive pulse generation circuit which generates a drive pulse (Fig. 2). The admitted prior art also teaches the provision of a reference clock signal, via reference clock wiring **6**, to control the driving of the image sensor (page 2 of the amendment, Paper No. 9, regarding Fig. 2). As the admitted prior art teaches the inputting of a clock signal from outside said drive pulse generation circuit chip (page 2 of the amendment, Paper No. 9, regarding Fig. 2; Fig. 2), the terminal for inputting the clock signal is also taught. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the practice of switching between control signals taught by Yasuda with the components of the admitted prior art to make a drive pulse generation circuit chip separate from the image sensing chip that multiplexes control signals to the image sensing chip. One of ordinary skill would have been motivated to

make such a modification to provide the possibility of driving the sensor in high or low resolution modes.

Regarding claim 21, Yasuda teaches first and second pulses from first and second control circuits (SSG1 **18** and SSG2 **19**) for reading out the signal from said image pickup portion in first and second modes (col. 4, lines 3-9). The admitted prior art teaches a drive pulse generation circuit for driving said scan circuit and a control signal from outside said semiconductor chip for controlling said drive pulse generation circuit (Fig. 2). The terminal that inputs the control signal is inherently taught.

Regarding claim 22, Yasuda teaches an image pickup apparatus comprising: a sensor chip comprising an image pickup portion (image pickup sensor **3**) including a plurality of pixels, which reads on the photoelectric conversion elements (col. 4, lines 19-23); a scan circuit (timing generator TG **21**) which reads out a signal from said image pickup portion (image pickup sensor **3**) (col. 4, lines 7-9); a first signal generation circuit (SSG1 **18**), which reads on the first control circuit, for generating a first control signal for reading the image sensor in a first mode, a second control signal coming from a second signal generation circuit (SSG2 **19**), which reads on the second control circuit, for reading the image sensor in a second mode, and a switch (SW **20**) which effects switching so that the image signals are read out from the image pickup sensor on the basis of one of the first control signal and the second control signal (col. 4, lines 3-9, and Fig. 1).

Yasuda does not teach a sensor chip formed on a single semiconductor substrate, a drive pulse generation circuit which generates a drive pulse for driving said scan circuit, the use of reference clocks for controlling the driving of the image sensor, a terminal which inputs a second

reference clock signal from outside said semiconductor substrate, or a control circuit provided externally to said semiconductor substrate and effects control so that said drive pulse generation circuit generates the second pulse. The admitted prior art does teach a sensor chip formed on a single semiconductor chip and a drive pulse generation circuit that generates a drive pulse for driving said scan circuit (Fig. 1). The admitted prior art also teaches the provision of a reference clock signal, via reference clock wiring **6**, to control the driving of the image sensor (page 1, lines 11-15). As the admitted prior art teaches the inputting of a clock signal from outside said sensor chip (page 1, lines 10-15; Fig. 1), the terminal for inputting the clock signal is also taught. The admitted prior art also teaches a control circuit (microcomputer 2) provided externally to said semiconductor substrate that effects control over the reading of the image sensor (Fig. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the practice of switching between control signals taught by Yasuda with the components of the admitted prior art to make an image sensing apparatus that multiplexes control signals coming from both on- and off-chip sources to drive the image sensor in a plurality of modes. One of ordinary skill would have been motivated to make such a modification to provide the possibility of driving the sensor in high or low resolution modes.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dorothy Wu whose telephone number is 703-305-8412. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-7644.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703)306-0377.

Dorothy Wu
DW
August 12, 2003

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600